Semiconductor Manufacturing And Advanced Research With Twins Usa Institute

New CHIPS R&D Initiative – Semiconductor Manufacturing and Advanced Research with Twins

Victor Zhirnov)
Chief Scientist
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The 19th U.S.-Korea Forum on Nanotechnology, Kintex, Gyeonggi-do, , July 3 & 4, 2025

Outline

- State of microelectronics in 2025-2030
- Semiconductor manufacturing x.0
- SMART USA Institute

SRC's Plan for the Decade

The What

2021
2030 Decadal Plan for Semiconductors

The How

2023
Microelectronics & Advanced Packaging Technologies (MAPT) Roadmap

Implementation

2025- 2030
Operation of SMART USA Manufacturing USA Institute

State of microelectronics in 2025-2030

Needs: Decadal Plan for Semiconductor

Drivers: MAPT Roadmap

- Artificial Intelligence **Key Driver**
- Automotive,
- HPC, mobile, communication, biomedical, & security

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CoPilot generated image

- Prompt: *draw sustainability picture with PFAS, renewable power, green house gases, compute energy efficiency as main themes*
- Content credentials - **Generated with AI**
- 1.35kWH used to generate this picture ~ 18s

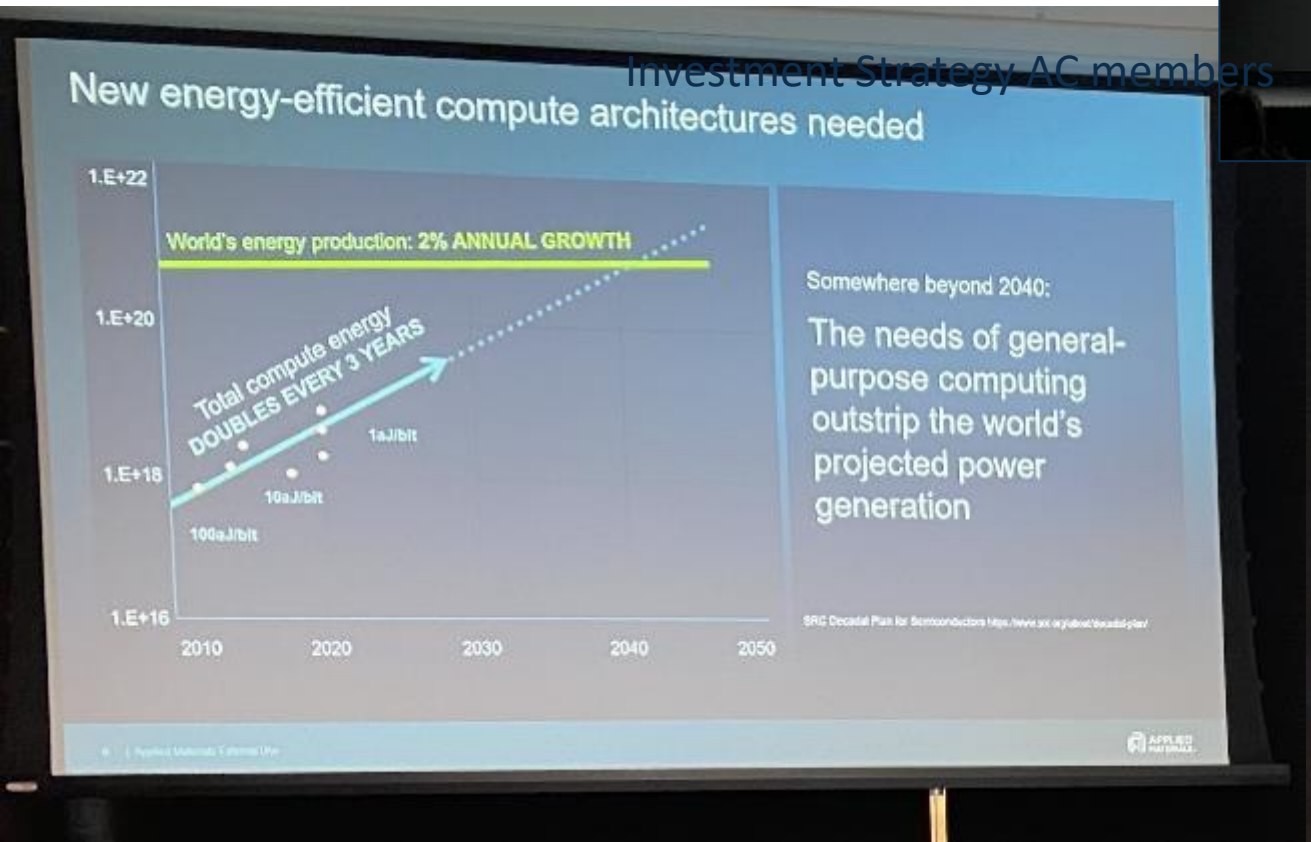
$$\sim \frac{5 \cdot 10^6 J}{18s} \sim \frac{300,000W}{100W / chip} =$$

$$= 3000 \quad chips$$

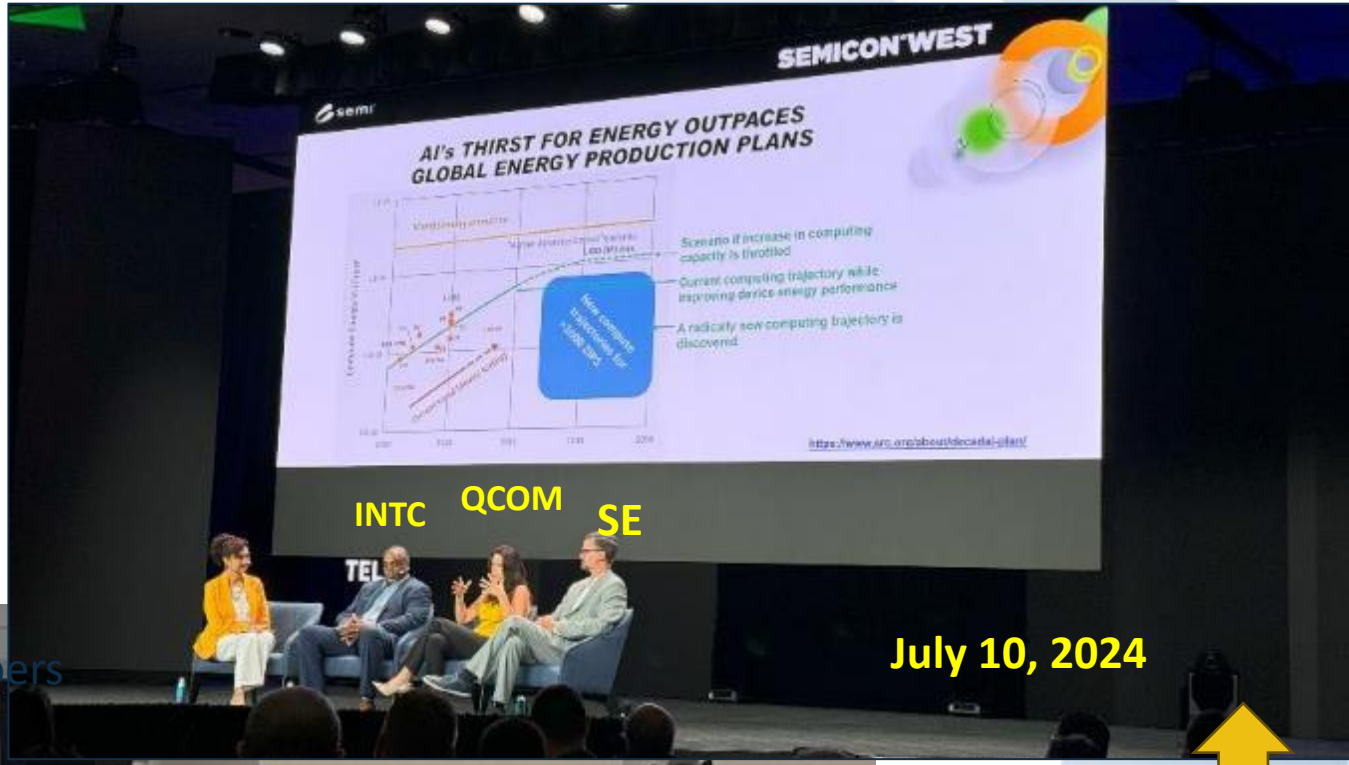
Takeaway message: This is a LOT of energy!

Big Energy

Takeaway message:
Energy is a big and rapidly growing problem for ICT



Investment Strategy AC members



July 10, 2024

September 23, 2024

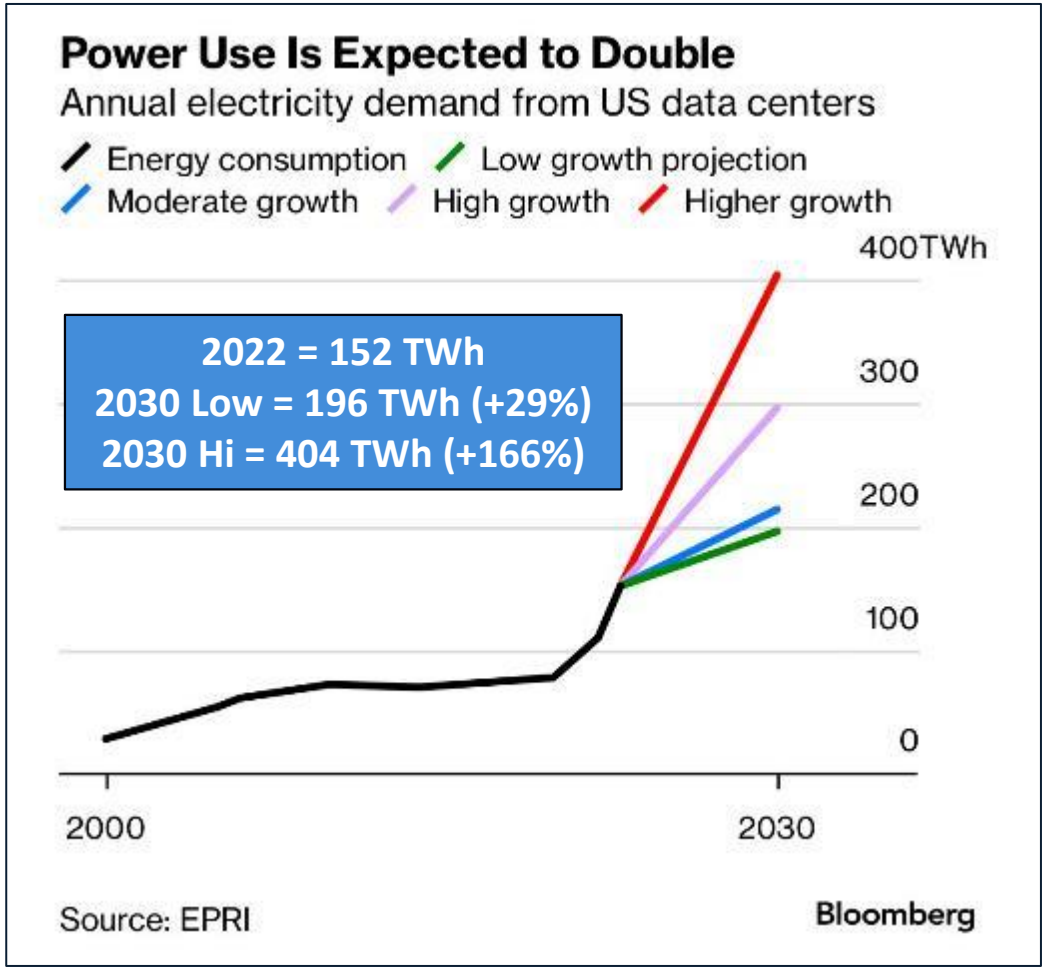
Big EnergyChief Sustainability Officer (CSO) Panel Discussion – Bracing for the Evolving Global Risk for the Semiconductor Ecosystem

CTO of Applied Materials Om Nalamasu presents his keynote at the 18th U. S. – Korea Forum on Nanotechnology

Sam Altman's AI Position to USG - "Infrastructure Is Destiny"

- At a White House meeting in Sept 2024, Altman made a plea for AI: **we need more energy—fast**
- EPRI - "data centers by 2030 will use as much as **9.1%** of all electricity generated in the US, compared with **4%** today."
- Goldman Sachs - "47GW of incremental power generation capacity will be required to support US data center demand growth through 2030."
- Such a capital investment would be **~$50 Billion**.

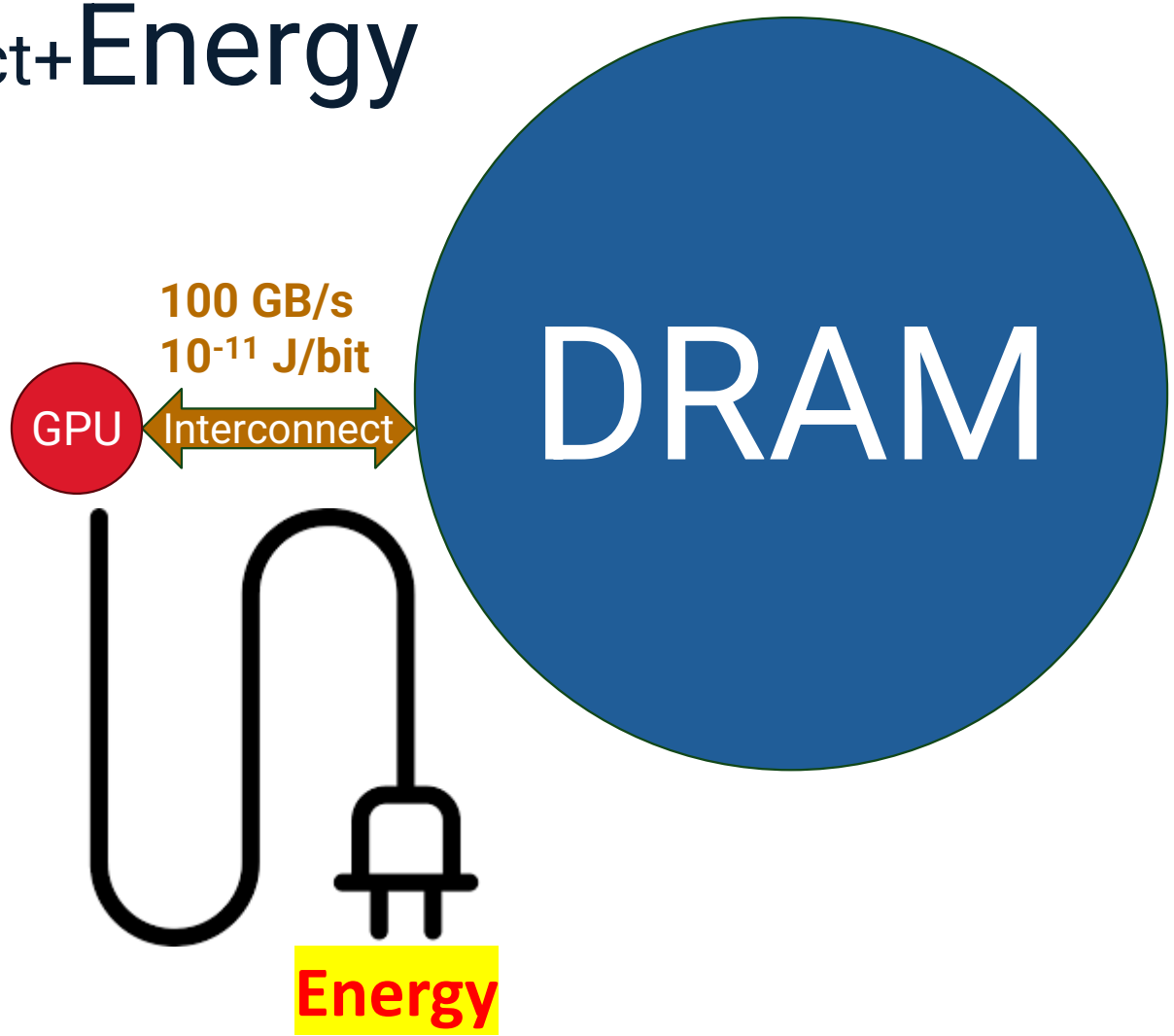
➢ The **Stargate Project**, incorporated in Delaware as Stargate LLC, plans on investing up to **US $500 billion** in AI infrastructure in the United States by 2029



https://www.bloomberg.com/news/articles/2024-10-17/sam-altman-s-energy-new-deal-is-good-for-openai-and-ai-what-about-americans
Stargate LLC - Wikipedia

What is AI (now)?

AI=GPU+DRAM+Interconnect+Energy



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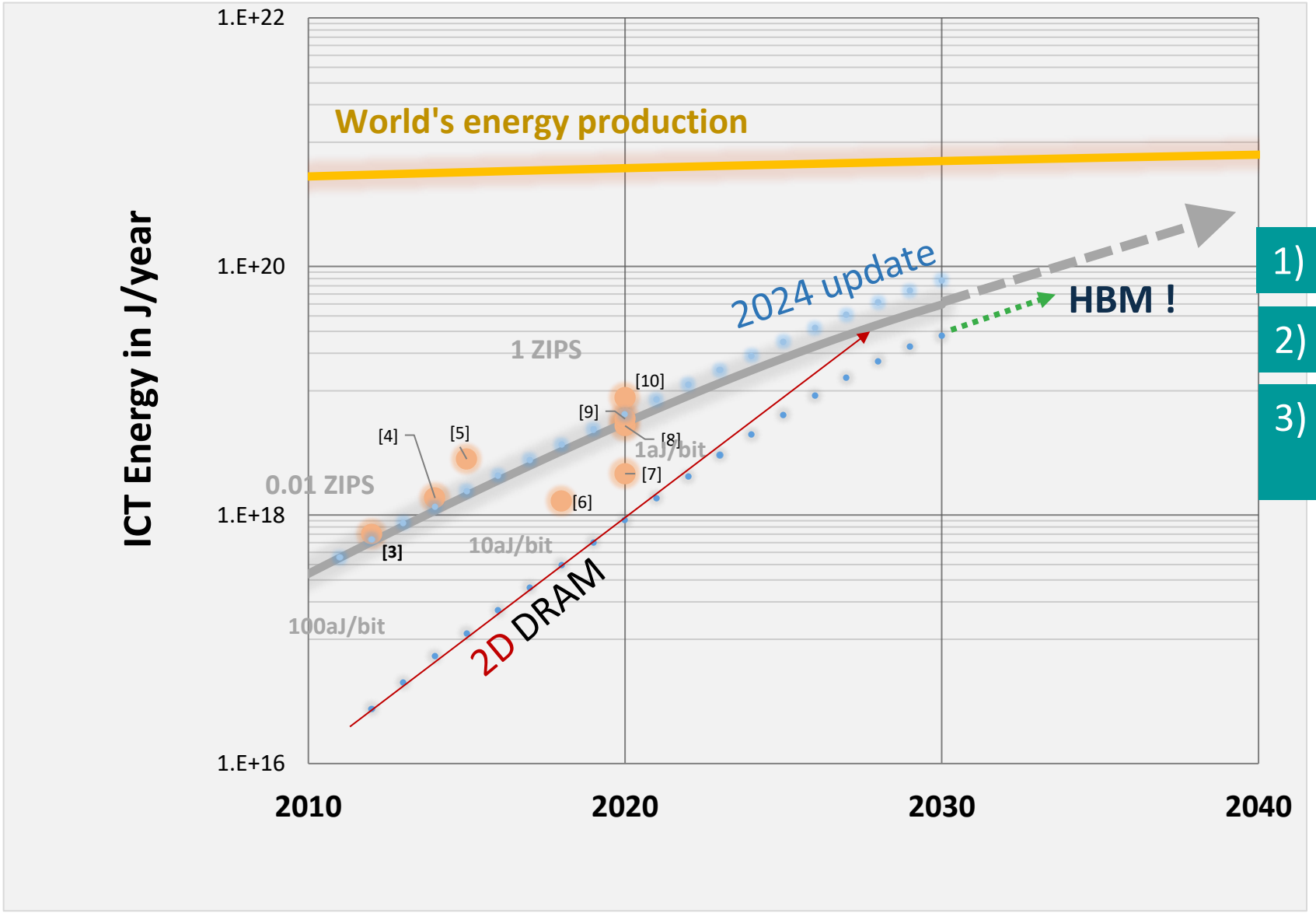
ICT Energy (computation)

Source: Decadal Plan



Takeaway messages:

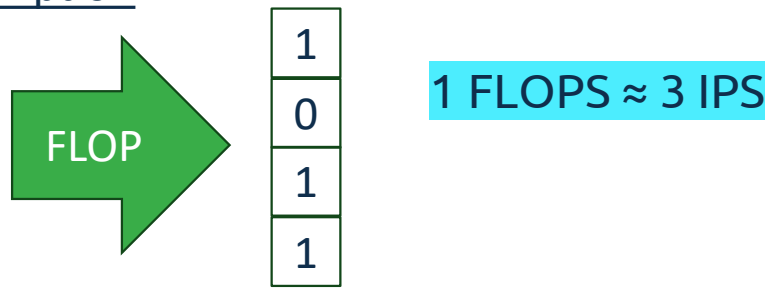
1) A validation of the 2021 model

2) The model is correct

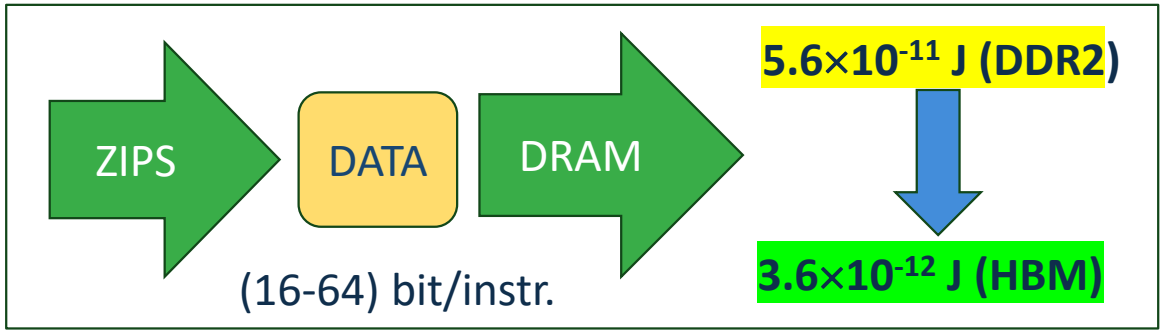
3) Transition to 3D seems to ease the energy problem

DRAM is used to support computation

Assumption

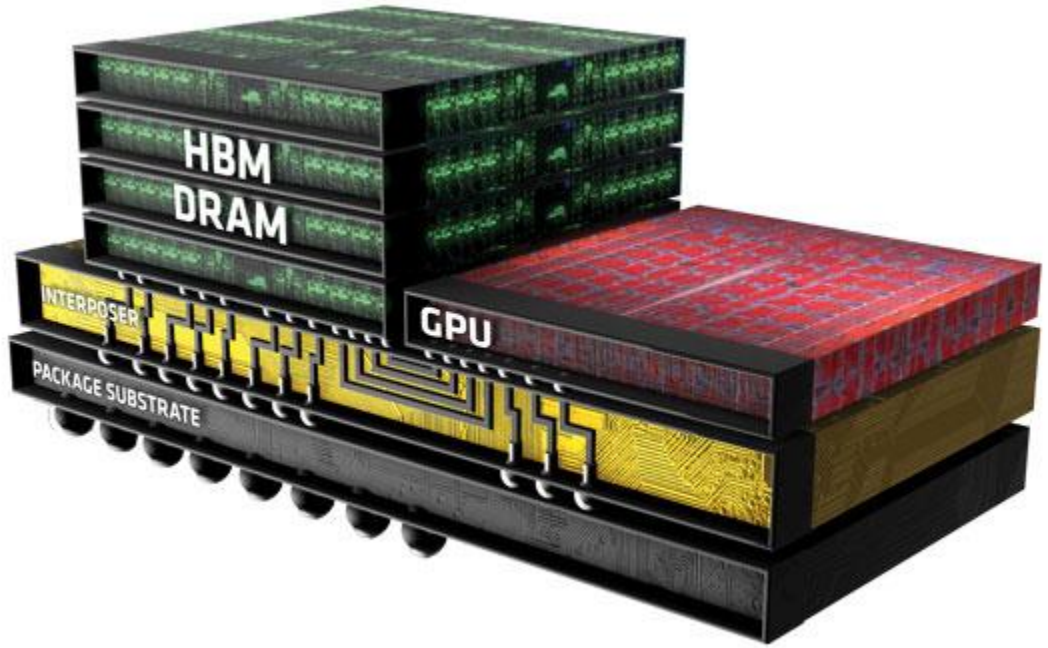


1 FLOPS ≈ 3 IPS



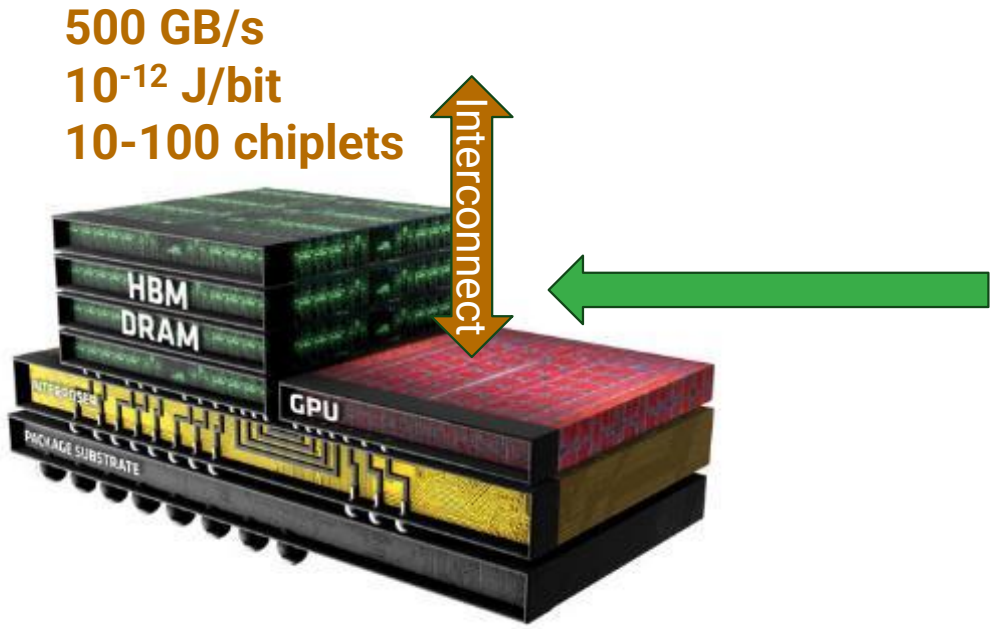
DRAM energetics

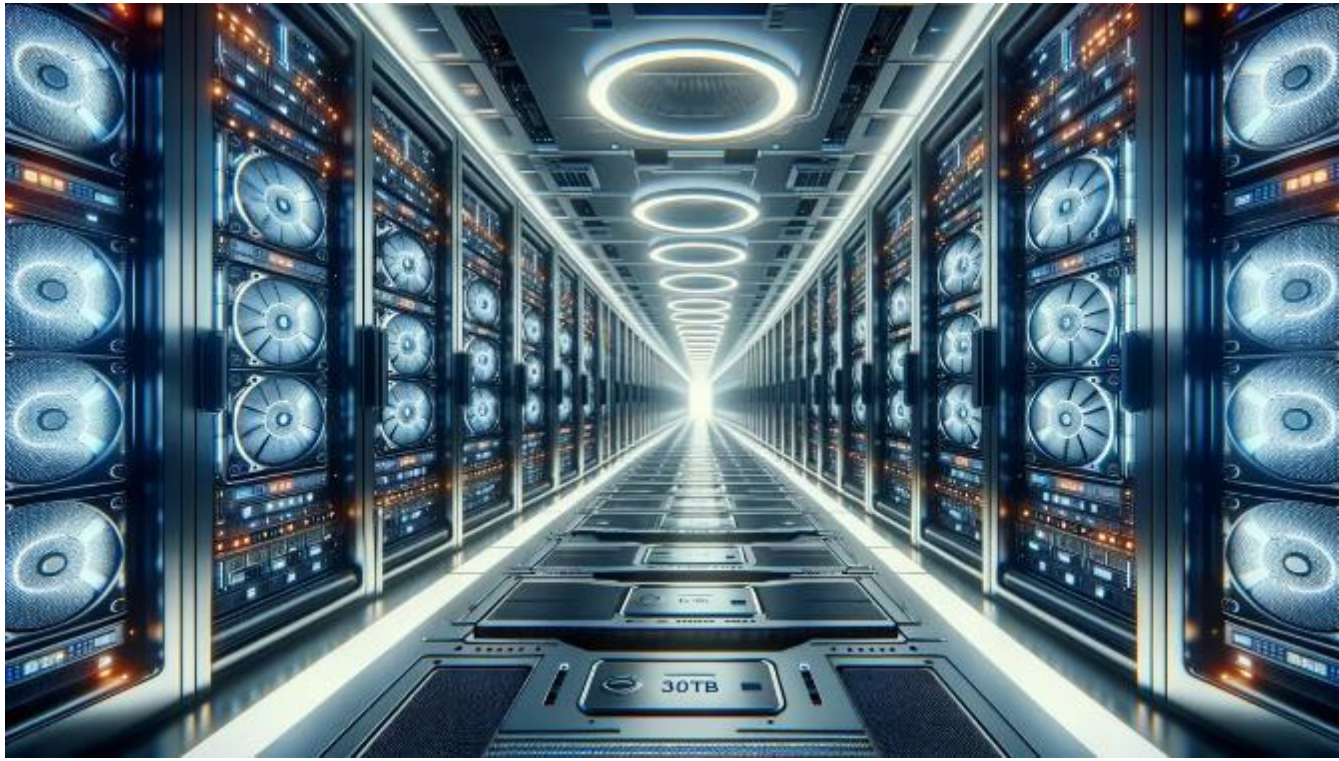
	AMD Radeon R9 290X	NVIDIA GeForce GTX 980 Ti	AMD Radeon R9 Fury X	Samsung's 4-Stack HBM2 based on 8 Gb DRAMs	Theoretical GDDR5X 256-bit sub-system
Total Capacity	4 GB	6 GB	4 GB	16 GB	8 GB
Bandwidth Per Pin	5 Gb/s	7 Gb/s	1 Gb/s	2 Gb/s	10 Gb/s
Number of Chips/Stacks	16	12	4	4	8
Bandwidth Per Chip/Stack	20 GB/s	28 GB/s	128 GB/s	256 GB/s	40 GB/s
Effective Bus Width	512-bit	384-bit	4096-bit	4096-bit	256-bit
Total Bandwidth	320 GB/s	336 GB/s	512 GB/s	1 TB/s	320 GB/s
Estimated DRAM Power Consumption	30W **1.2×10^{-11} J**	31.5W **1.2×10^{-11} J**	14.6W **3.6×10^{-12} J**	n/a	20W **7.8×10^{-12} J**



What is AI (soon)?

AI=GPU+HBM+TSV+Heat+3DPackage+3DNAND





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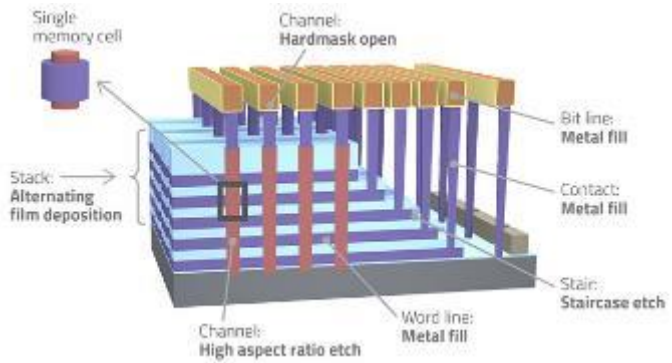
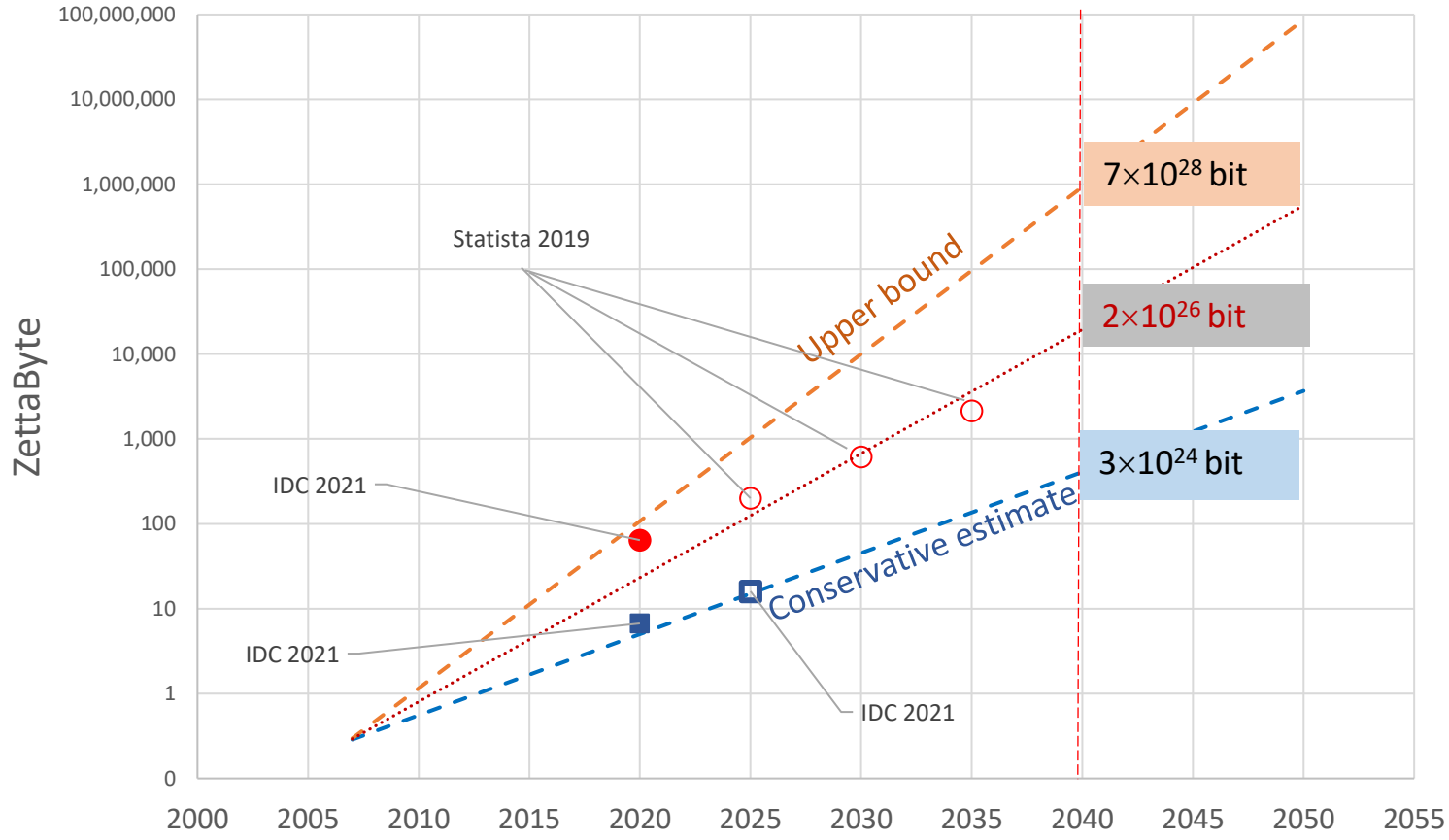
Data Storage in the AI Era

- With the growing value of data in the AI ecosystem, flash data storage (**3D NAND**) is emerging as an invaluable asset
  - Speed+scalability

3D NAND



Source: Decadal Plan



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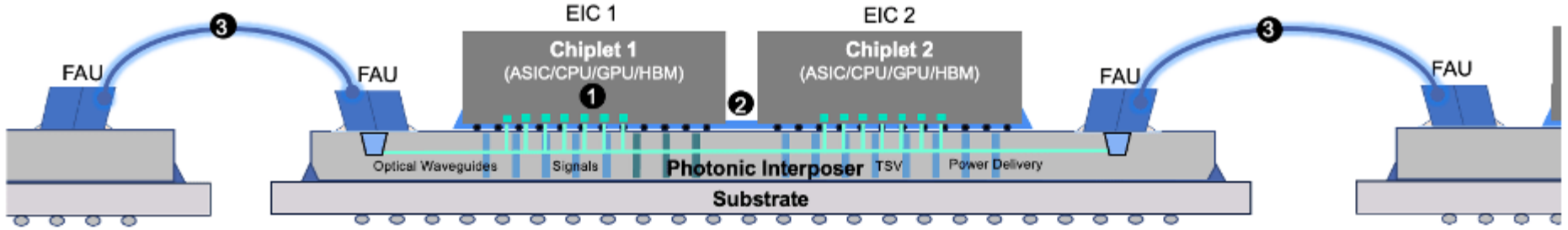
What is AI (future)?

Advancing AI with photonic system integration

AI=GPU+HBM+**CPO** Heat +3DPackage

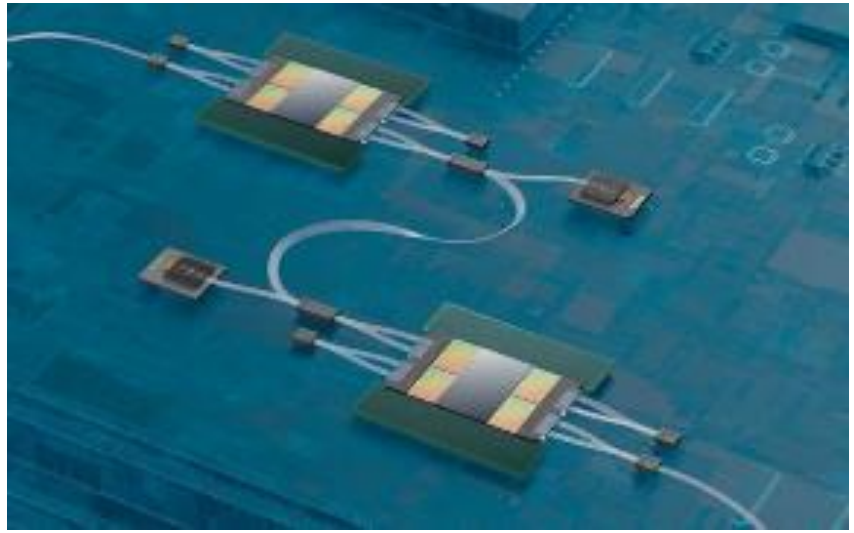
co-packaged optics



Source: Celestial AI

>1000 GB/s
<10^{12} J/bit
1000 chiplets

Photonic Interconnectc, I/Os



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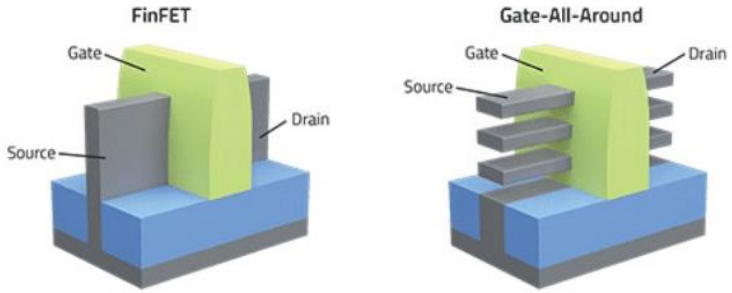
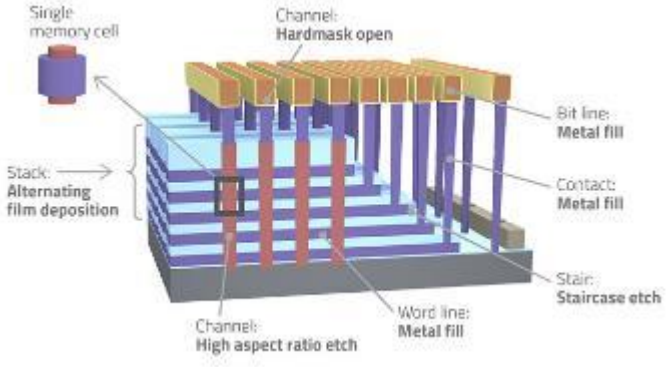
3D Challenges

3D Logic



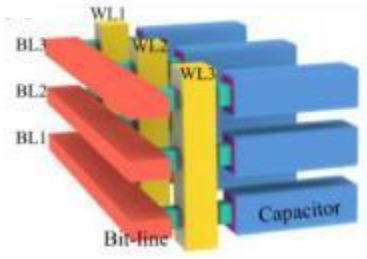
Lam Research

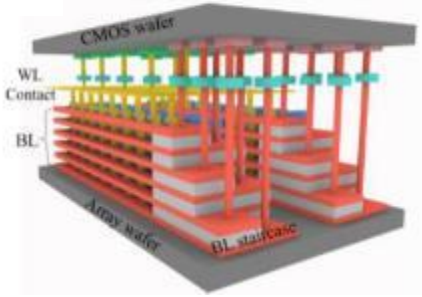
3D NAND



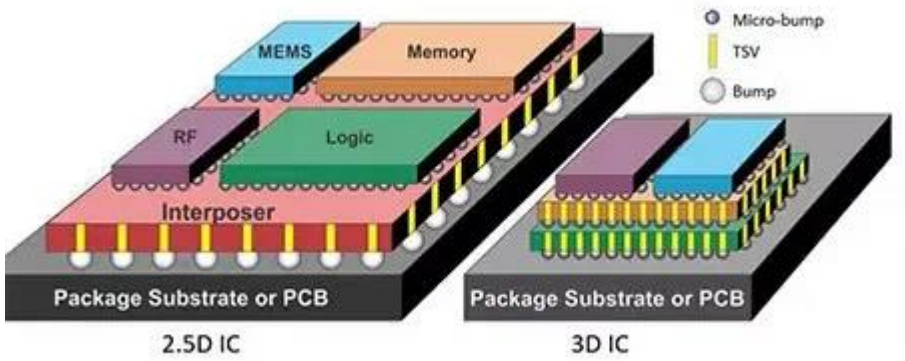
www.businesskorea.co.kr/news/articleVie

3D DRAM





Advanced Packaging

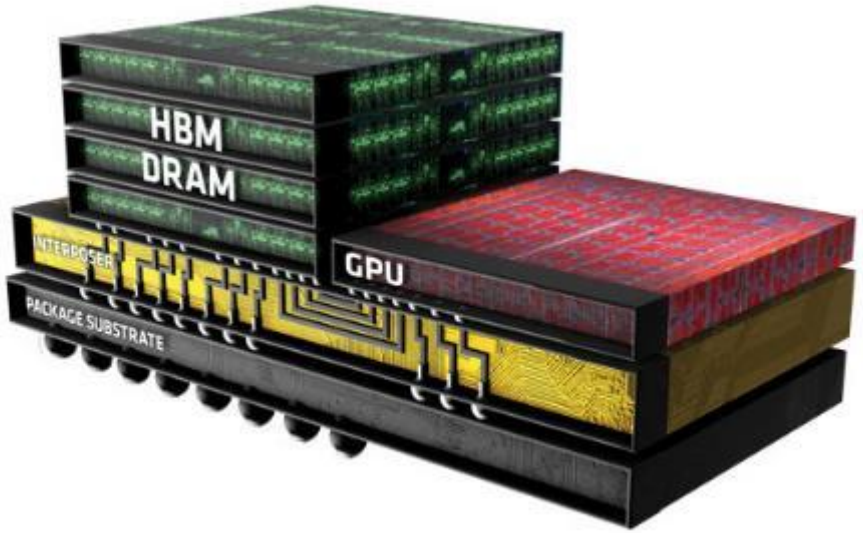


Siemens EDA

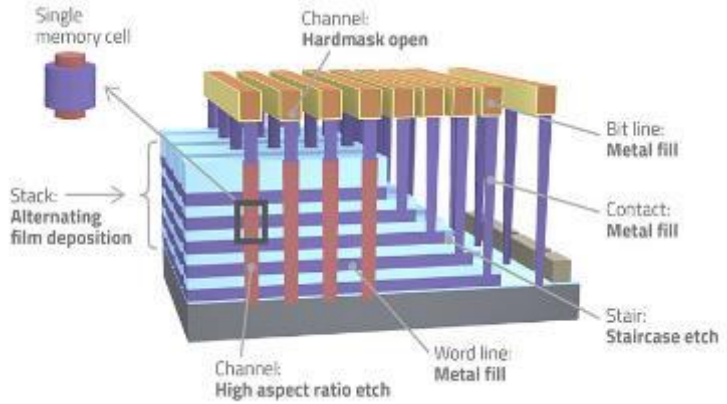
- 3D at device, die and package
- Nano-scale with coverage and throughput
- Dimensional, compositional and property measurements

What are Challenges for AI?

AI=GPU+HBM+TSV+3D Package +Heat +3DNAND



3D NAND



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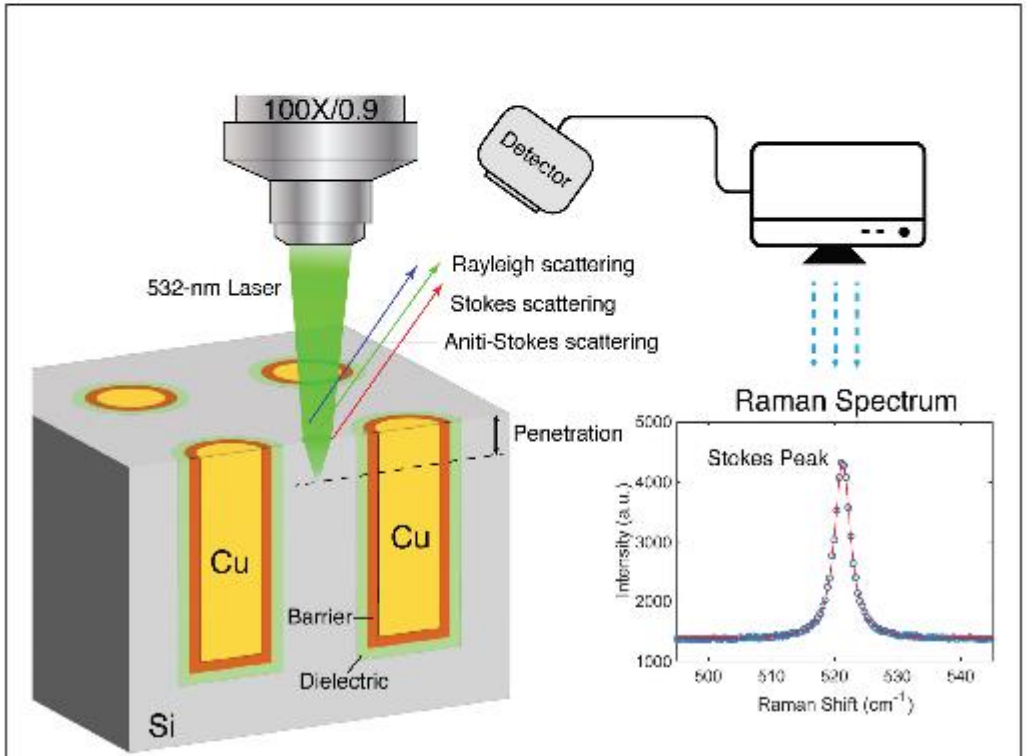
Journal of Applied Physics

AIP Publishing

Vol. 137, Iss. 8, 28 Feb. 2025

Scaling effects on the microstructure and thermomechanical response of through silicon vias (TSVs)

Shuhang Lyu, Thomas Beechem, and Tiwei Wei



Available Online: pubs.aip.org/aip/jap

Result from recent SRC research

Needed:

interconnect density >10^6/mm^2 ⇒TSV dia. <1μm

Problem: Heat

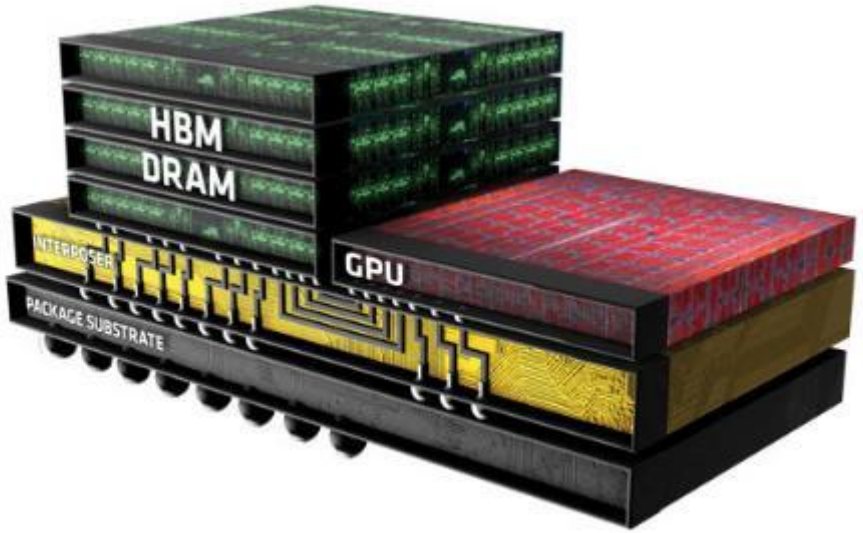
e.g. thermomechanical stress

Metrology:

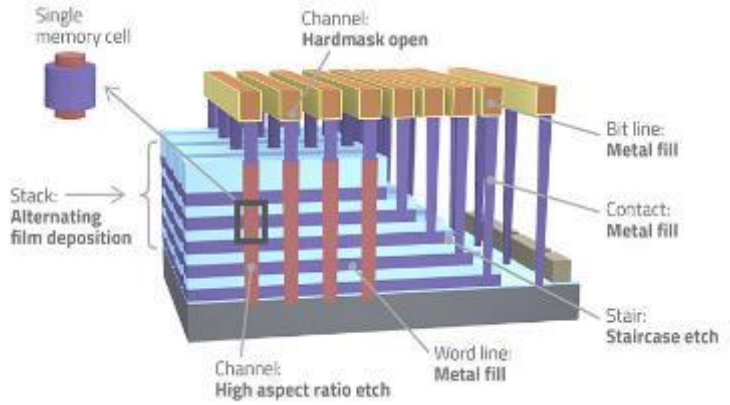
- Raman spectroscopy
- Electron Backscatter Diffraction

What arw Challenges for AI?

AI=GPU+HBM+TSV+3D Package +Heat+3DNAND



3D NAND



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Detection of defective chips from nanostructures with a high-aspect ratio using hyperspectral imaging and deep learning

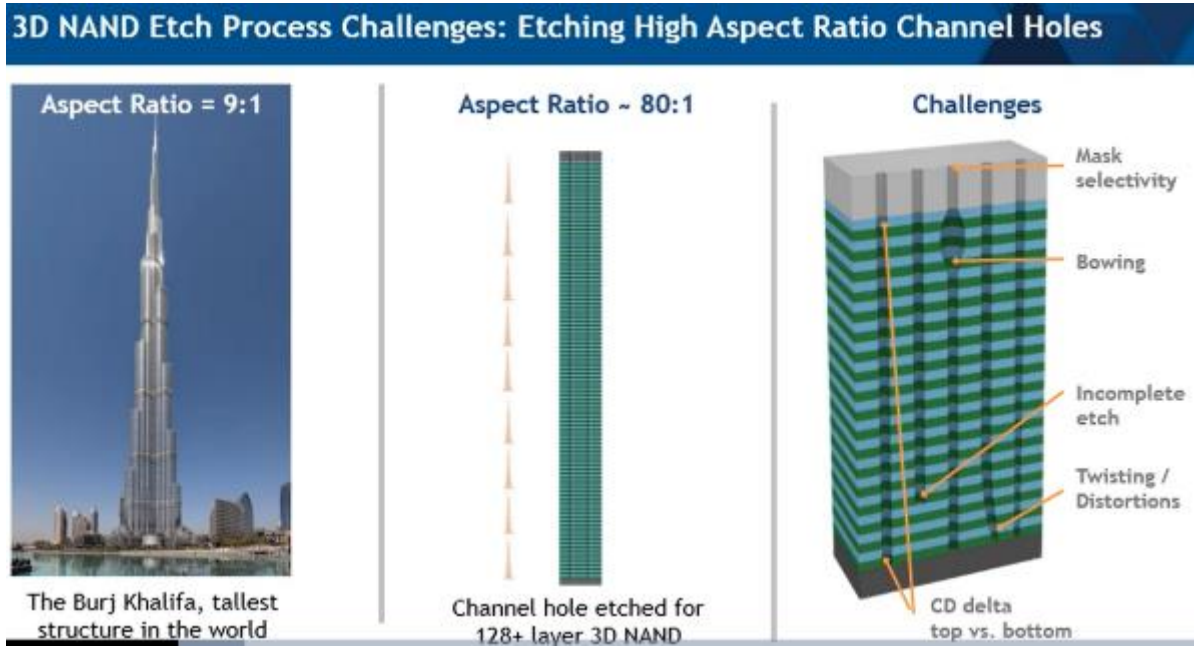
JM3 Journal of Micro/Nanopatterning, Materials, and Metrology

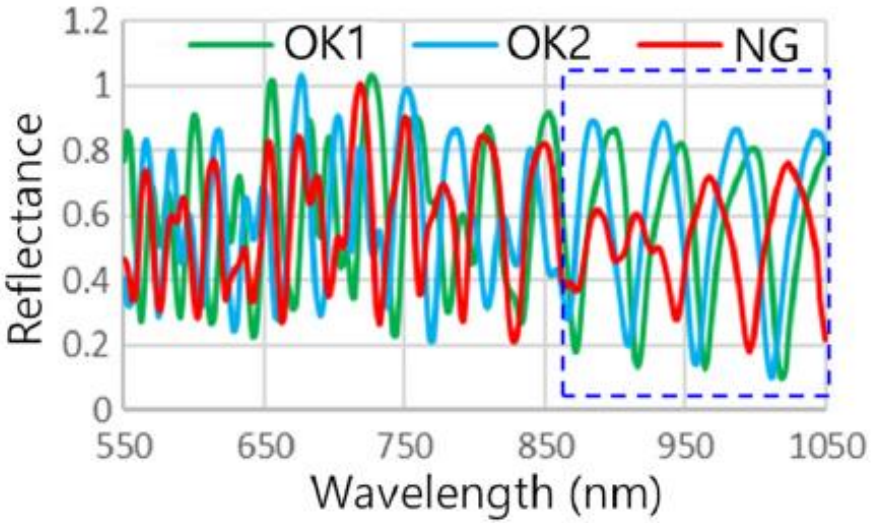
Oct–Dec 2024 • Vol. 23(4)

Sunhong Jun,[a,*] Wonjun Choi,[b] Yong-Ju Jeon,[b] Jeongsu Ha,[b] Kyuhwan Kim,[b] Sungyoon Ryu,[a] Myungjun Lee,[b] Yongdeok Jeong,[a] and Younghoon Sohn[a,*]

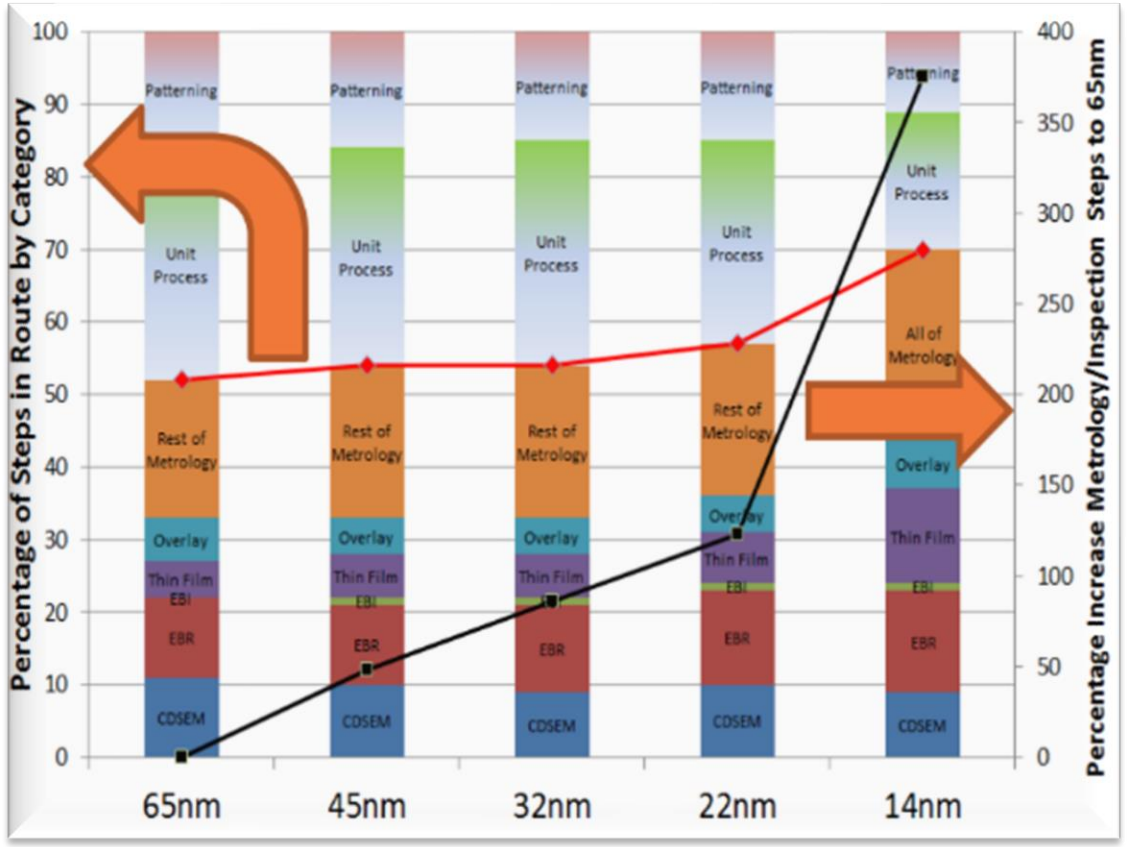
[a]Samsung Electronics Co., Ltd., Metrology and Inspection Technology Team, Hwaseong-Si, Republic of Korea
[b]Samsung Electronics Co., Ltd., Advanced Process Development Team 4, Hwaseong-Si, Republic of Korea

Imaging spectroscopic reflectometry (ISR)=Hyperspectral Imaging + Deep Learning





Fab Metrology Challenge



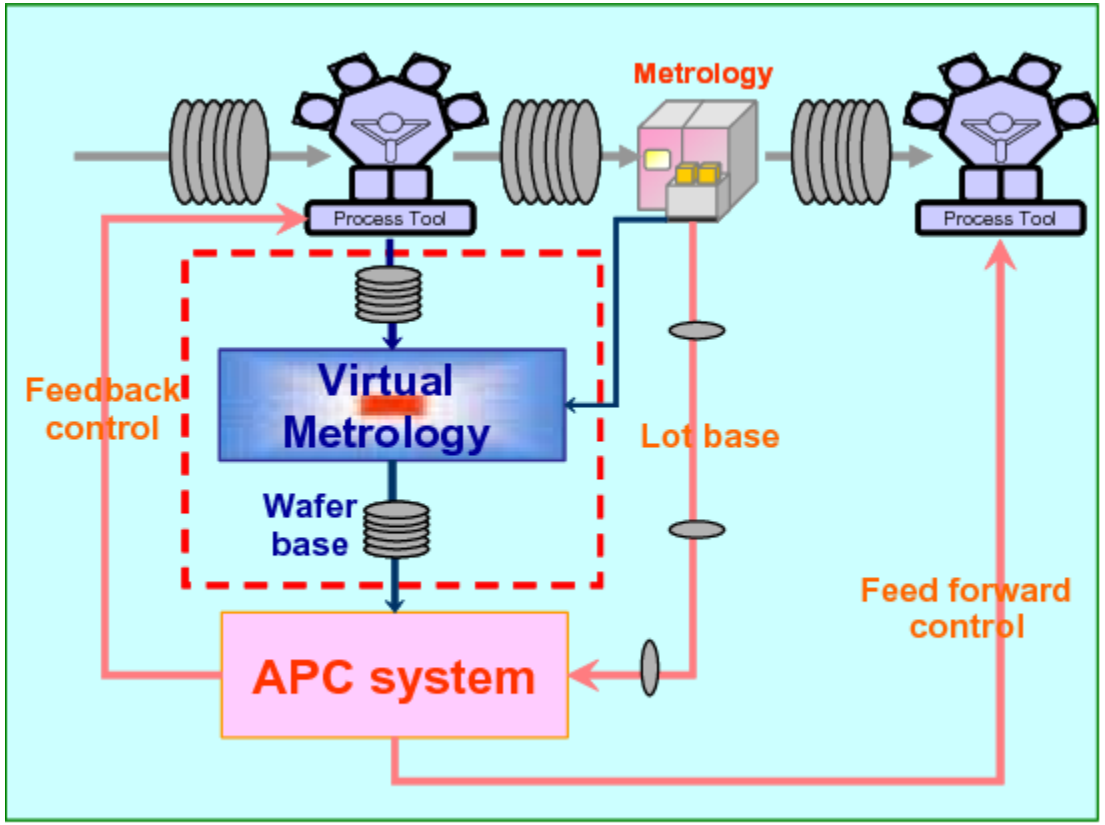
Alok Vaid (GF) FCMN 2019

- 50+% of fab process steps involve metrology
- Capex growing rapidly → 20+% of fab cost
- CD metrology/film thickness/defect inspection toolsets Off-line yield/product debug equipment is also required
- Emerging new materials/devices are driving needs for new capabilities

Source: Markus Kuhn / Rigaku, AVS 70 – Characterization and Metrology for MAPT Roadmap

A Call for Digital Twin Infrastructure

- Supports virtual metrology in semiconductor manufacturing



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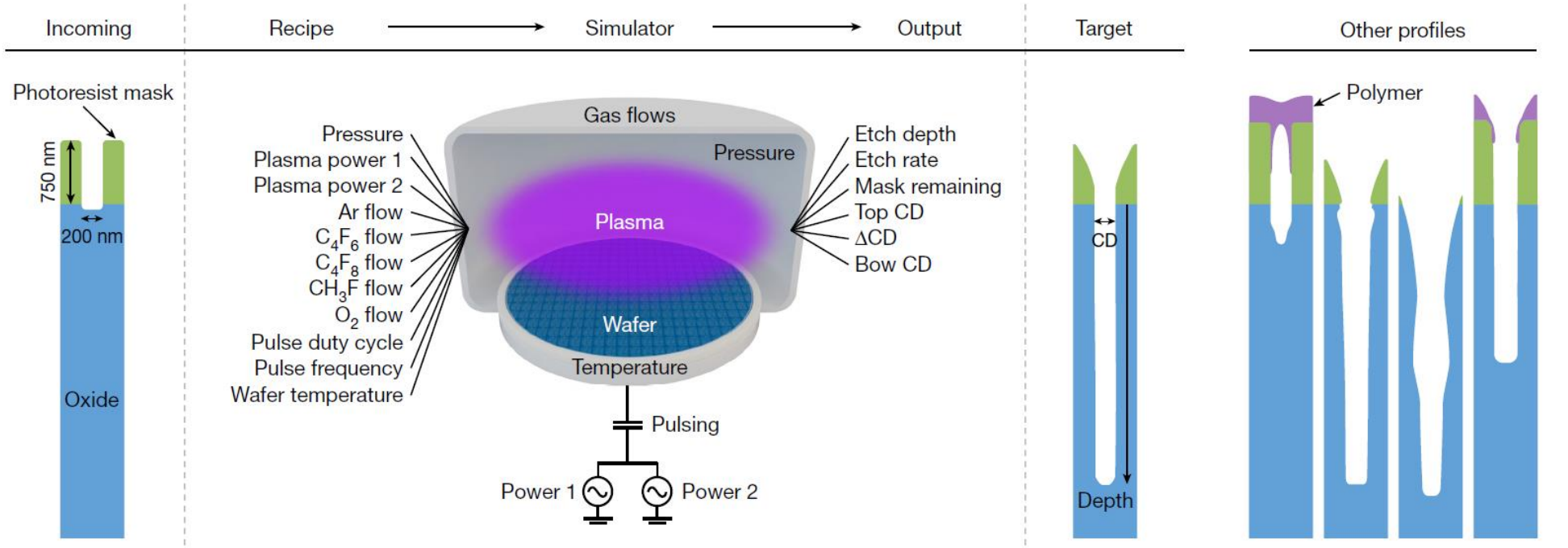
Article

Human–machine collaboration for improving semiconductor process development

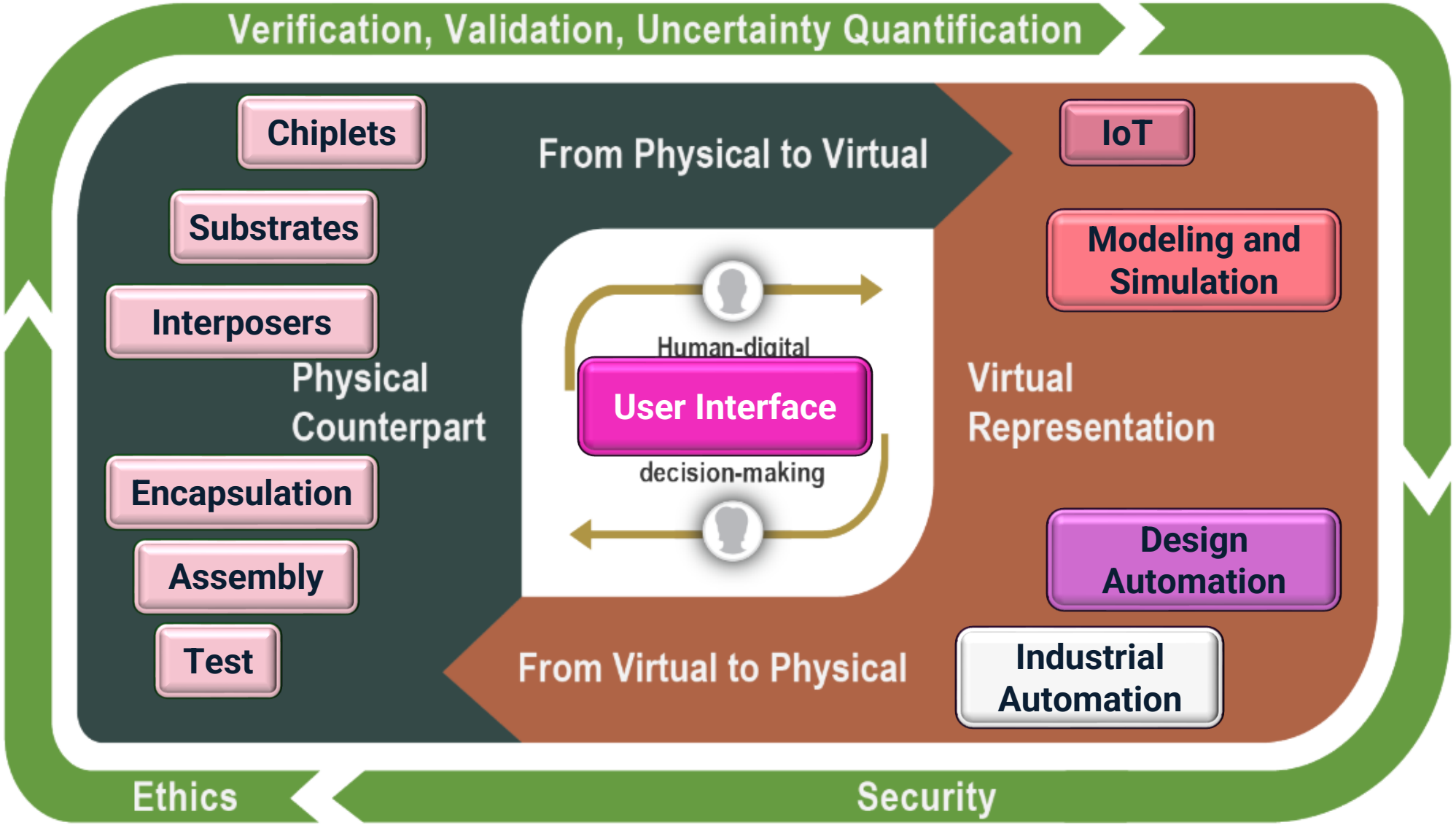
Nature | Vol 616 | 27 April 2023

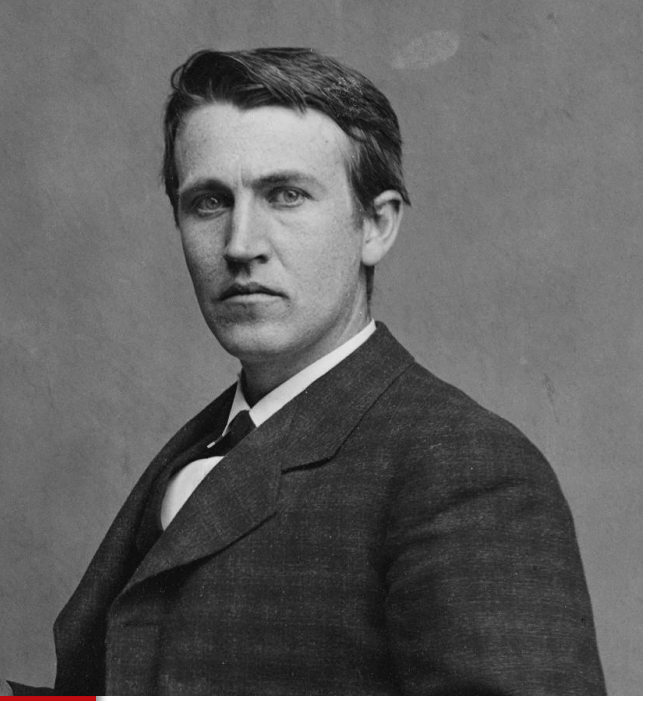
Keren J. Kanarik[1], Wojciech T. Osowiecki[1], Yu (Joe) Lu[1], Dipongkar Talukder[1], Niklas Roschewsky[1], Sae Na Park[1], Mattan Kamon[1], David M. Fried[1] & Richard A. Gottscho[1]✉



50% cost reduction!

A Digital Twin is More Than Just Simulation and Modeling





Thomas Edison

Master of rapid innovation development

Materials discovery:
Edison did use hunt and try extensively. He tested about 6,000 filament materials for the light bulb

Data driven: *"When I want to discover something, I begin by reading up everything that has been done along that line in the past… I gather **data** of many thousands of experiments as a starting point, and then I make thousands more."*

Application Space Exploration: Edison invented by repeatedly trying devices in more complex environments to progressively approximate their final use conditions.

SMART USA CHIPS Manufacturing Institute

SMART USA Award - Durham, NC Nov. 19th, 2024

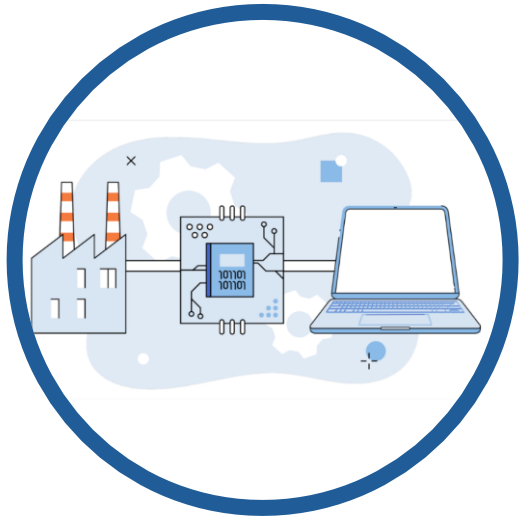
- A historic moment!
- Operated by SRC, SMART USA builds upon SRC's history of impact.
- Drives a **smart digital twin backbone** and manufacturing R&D, EWD for both chips and packaging.
- The 18th Manufacturing USA Institute.
- A key pillar of CHIPS Act - R&D.
- Combined total investment $1B/5-years with $285M in federal funding.

SRC

Digital/Physical Twin components of SMART proposal

- SMART = Semiconductor Manufacturing and Advanced Research with Twins
  - Digital Twin is a tool to accelerate both R & D and production
  - The Digital Twin component of the proposal can be:
    - Creating Digital Twins, grounded on physical
    - Using Digital Twins (interfaced with physical)

SMART USA Objectives



SMART USA will convene stakeholders from across the semiconductor design, manufacturing, advanced packaging, assembly, and test sectors.

Within five years, we will:

- Collaboratively address shared challenges relevant to digital twins
- Reduce U.S. chip development and manufacturing costs by >40%
- Reduce manufacturing development cycle times by ≥35%
- Train and educate >110,000 people

Digital Twin Institute Approach

A physical facility and digital framework, integrated with industry-led research projects

1 Establish a **shared physical facility**

Expected activities:
- Baseline facility testbed
- Digital emulation hardware
- Core technical & operations staff

2 Competitively fund **industry-led technical and workforce development projects**

Deliver technical solutions, de-risk new tools, and conduct data analysis

Develop and test education & workforce development tools enabled by digital twins

3 **Digital framework** for interoperable data and models

4 Create a **shared marketplace** of digital twin models

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https://www.nist.gov/chips/chips-america-webinars

Elements of SMART USA

R&D

Digital Twins Technical Areas (DTTAs)

Semiconductor Manufacturing Technology (SMTASs)

Packaging Assembly Test Areas (PATAs)

Standards, SMART Marketplace & Backbone

Facilities & Computational Resources

Education and Workforce Development

Infrastrucure

SMART USA Members

Broad Adoption

- Reduce Costs
- Improved Speeds
- Security Assurance

Conclusions

- “Overnight,” packaging and heterogenous integration has became “cool again” as a recognized competitive advantage.
- Metrology is key enabling capability for meeting current and future semiconductor technology and manufacturing requirements
- We need to develop precise, accurate, fast 3D tools, simulations, and design techniques that that operate at the “mesoscale.” **Infuse ML/AI.**
- Cooperation, alignment and investment in fundamentals, nurturing lab to fab and overall ecosystem infrastructure are necessary → need to align academic, government and industry needs and capabilities
- The Decadal Plan and MAPT Roadmap are the guides to help enable this

We must lead in BOTH technology and workforce development to emerge as true frontrunners

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